## 1. Abbreviation:

ANSI: American National Standards Institute

DIO: Digital Input Output

E/O: Electrical to Optical

FAT: Factory Acceptance Test

FPGA: Field Programmable Gate Array

HMI: Human Machine Interface

HVPS: High Voltage Power Supply

JTAG: Joint Test Action Group

KRIA: Create Innovative Idea

LED: Light Emitting Diode

LVTTL: Low Voltage Transistor Transistor Logic

O/E: Optical to Electrical

PO: Purchase Order

POF: Plastic Optical Fiber

QA: Quality Assurance

RX: Receiver

SAT: Site Acceptance Test

SCU: Signal Conditioning Unit

SoC: System on Chip

SOM: System on Module

SPS: Switched Power Supply

TX: Transmitter

USB-UART: Universal Serial Bus- Universal Asynchronous Receiver/Transmitter

VITA: VMEbus International Trade Association

VME: Versa Module Eurocard

VPX: ANSI/VITA 46.0

Zynq: Word Created from Zinc

## 2. Introduction: HVPS Controller

Functionality of HVPS controller is to control a high voltage power supply, the main functions include,

    i. Control operation parameters and mode of operation.
    ii. Monitor and protect power supply.
    iii. Follow higher level controller.

Following block diagram shows proposed controller configuration.
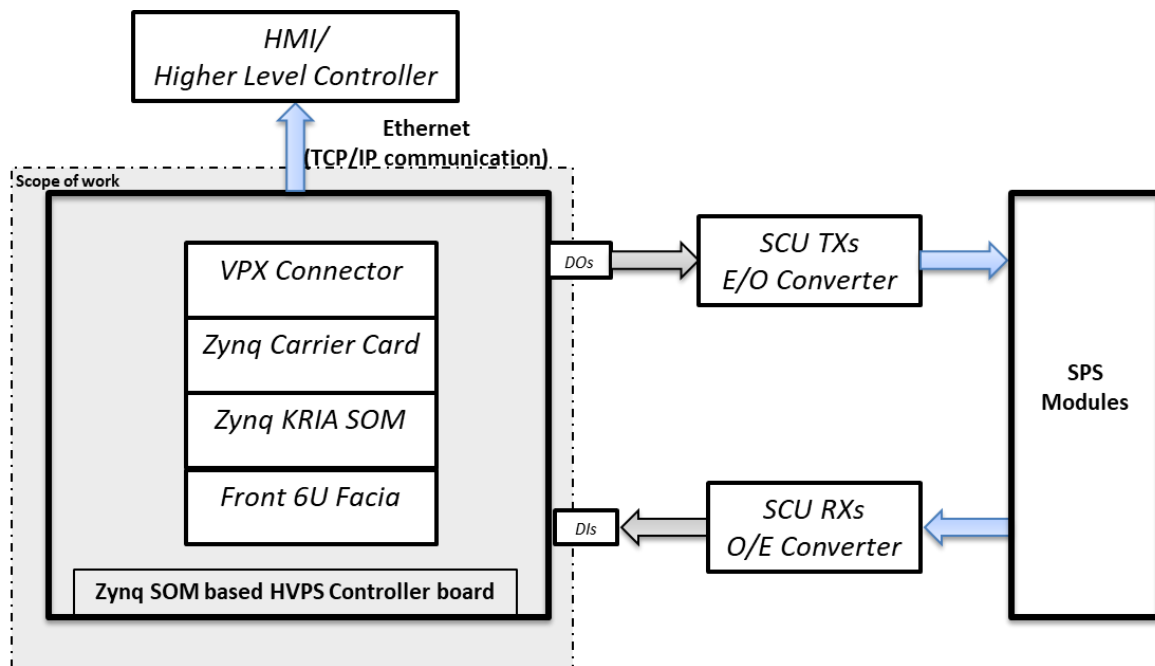
**Figure 1 Zynq SOM based HVPS Controller Configuration**

Supplier is to develop System on Module (SOM) based Zynq controller board. System on Module based Zynq controller should be compatible with 6U assembled controller bin provided by ITER-India, shown in Figure 2.
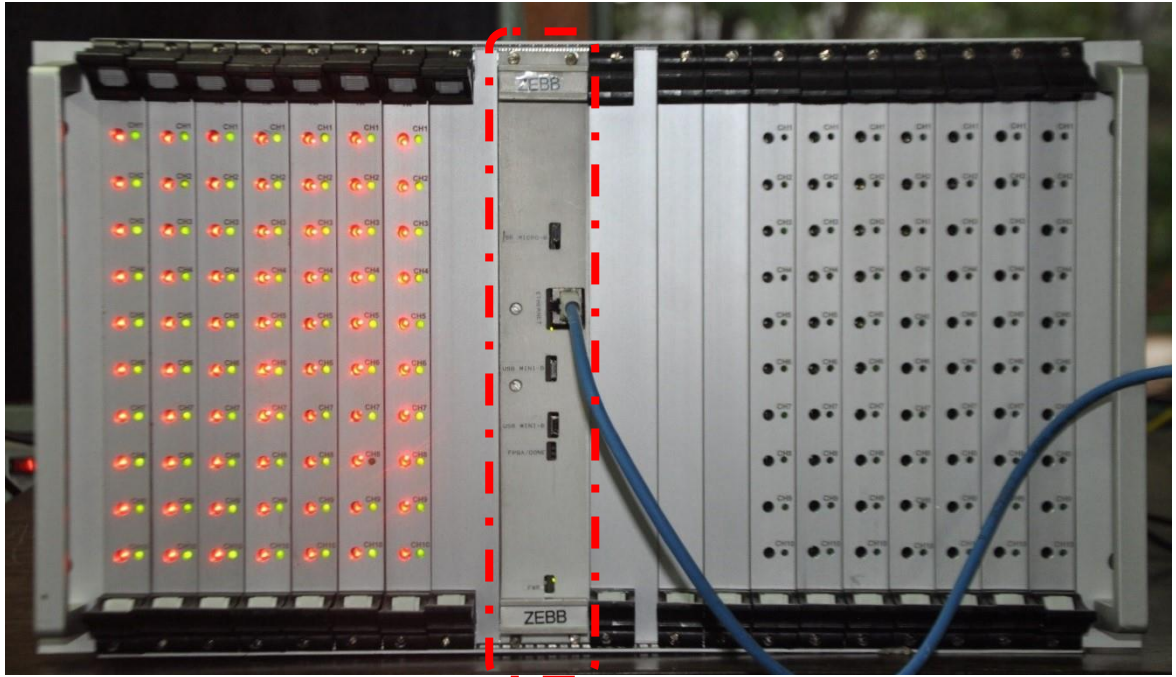
**Figure 2 CE certified assembled controller bin with Zynq SoC board integrated with
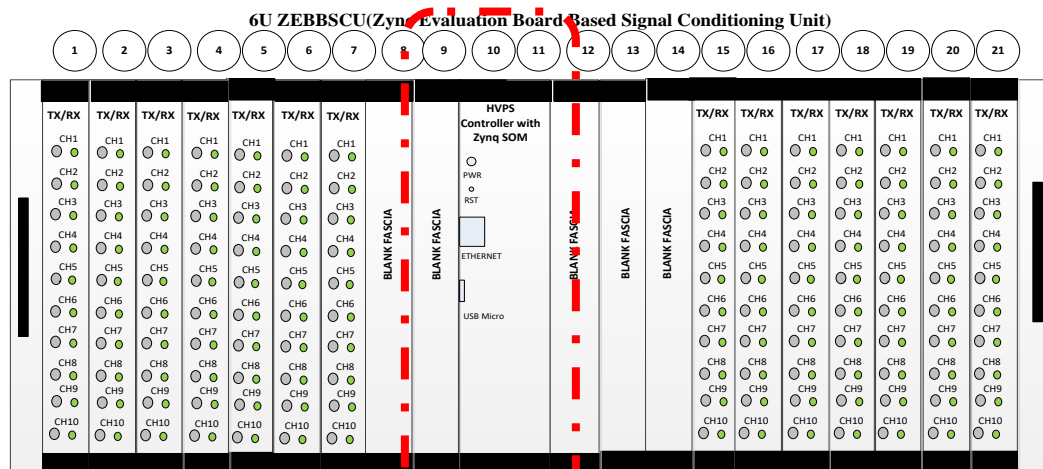signal conditioning cards**



**Figure 3 Proposed Zynq SOM based controller board to be retrofitted with Existing
6U controller bin**

## 3. Scope of Supply

Supplier shall develop and supply (1 Prototype + 3 Production) assembled controller board compatible with (to be housed in) existing 6U controller bin and retrofitted with mother board. Each HVPS controller board must consist of Zynq SOM board and carrier board. Each controller board shall be capable of providing functional support and compatibility to existing 6U controller bin.

Thus, a typical single HVPS controller board comprises of item mentioned in Table 1 Single HVPS controller board components,

**Table 1 Single HVPS controller board components**

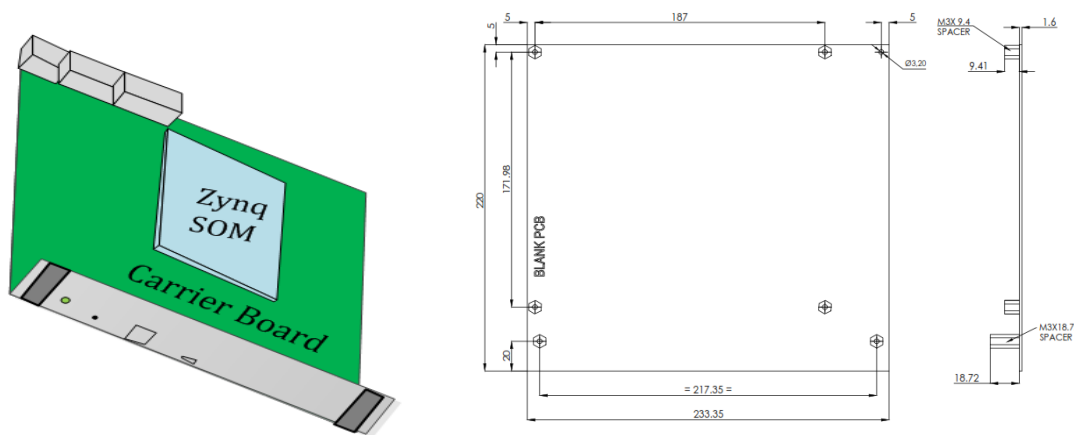| Sr. No. | Part Description | Quantity (Nos) |
|---------|------------------|----------------|
| 1 | Industrial Grade Zynq KRIA SOM | 1 |
| 2 | Carrier Board | 1 |
| 3 | 6U size Facia | 1 |
| 4 | VPX Connector for Carrier Board | 1 |

1. Node locked Vivado ML Enterprise Edition software licence for Windows 11 Operating System (Perpetual License in the name of ITER-India) - 1No

2. Design, Development, manufacturing of prototype Zynq SOM based HVPS Controller board - Prototype Unit (1 No)[1]

3. Zynq SOM based HVPS Controller board – Production Unit (3 Nos.)[2]

4. Test programs/ application software for loopback testing with provision to communicate to higher level controller and HMI through Ethernet (TCP/IP communication).

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[1] The controller board shall be compatible with existing 6U bin; 136 DIOs (LVTTL) of the controller shall provide/carry the signals to/from 136 SCU channels of the bin.

[2] Prototype Zynq SOM based HVPS controller shall be tested at ITER-India lab for functional performance with integration of all 136 DIOs.

Production to be initiated after receiving acceptance note for Prototype Unit from ITER-India.

**Technical Specifications for Zynq SOM based HVPS Controller Boards
(1 Prototype + 3 Production) with Vivado Software Licence**

ITER-India

**Figure 4 Proposed Design of Zynq SOM based Controller Board with Existing 6U Bin**
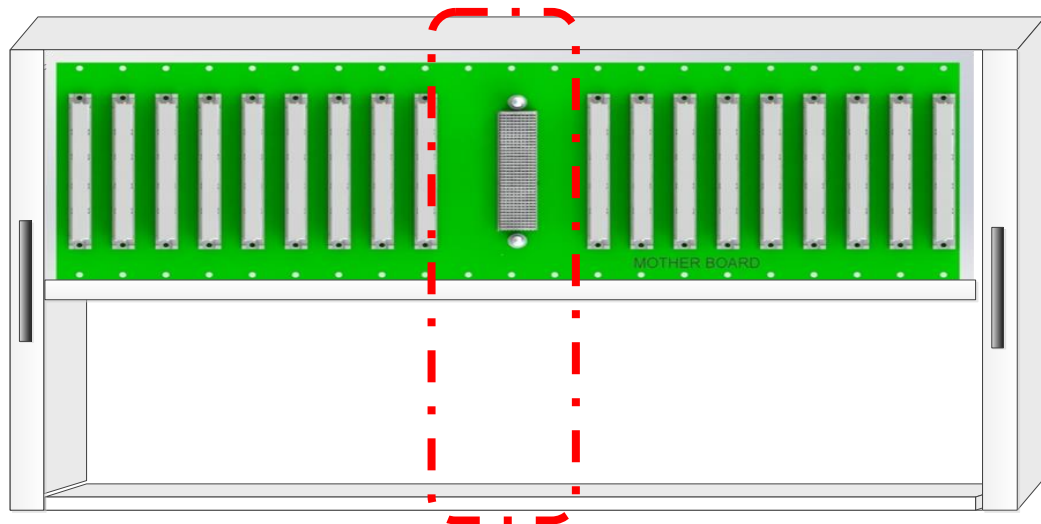


**Figure 5 Existing Motherboard with VPX Connector with Proposed location of Zyqn SOM based controller board**

## 4. Scope of work

1. Procurement of Vivado Node Locked ML Enterprise Edition software license for Windows 11 Operating System (Perpetual License in the name of ITER-India).

2. Procurement of Industrial Grade Zynq KRIA SOM.

3. Design of electrical, mechanical, firmware and power-on configuration of SOM carrier board.

4. Controller board should have provision to communicate to higher level controller and HMI through Ethernet (TCP/IP Communication).

5. Supplier shall provide VPX connector to interface carrier board with mother board.

6. In the existing 6U Bin DIs/DOs (with 3.3V & 0V for logic high & low respectively) to/from controller board are converted in to electrical/optical signals through

signal conditioning units (SCUs) receiver (RX)/transmitter (TX). 136 DIOs from SOM based Zynq controller board shall be compatible with existing 6U bin.

7. Submission of Design and test procedure documents (within 3 months from the date of PO) to ITER-India for approval;

   (1) Schematic drawing & PCB layout for Carrier board of Zynq SOM

   (2) Mechanical assembly drawing of a HVPS controller

   (3) Detailed bill of material

   (4) Detailed acceptance test procedure & plan for the tests specified under Section 6 (Test to be performed).

8. Development of test programs/ application software for loopback testing.

9. Development of first Prototype HVPS controller board compliant with 6U bin assembled with SCU cards (Tx/Rx) and mother board. Functional test according to test matrix and submission of test reports to ITER-India for review and approval.

10. Supply of prototype Unit to ITER-India Site. Supplier representative shall come to ITER-India site for SAT of prototype.

11. After getting approval for Prototype HVPS controller board, manufacturing of remaining three HVPS controller boards.

12. Tests to be performed at supplier site in presence of ITER-India representative in accordance with Test Matrix. Prepare test report and submit to ITER-India, approval of the same shall be the clearance for dispatch.

13. Supply of Production Units (3 Nos.) of HVPS controller board to ITER-India site along with deliverable documents.

14. Deliverable documents:

    i.   Test report for all HVPS controller boards in accordance with test matrix.

    ii.  As built schematic, assembly drawings and BOM (bill of material).

    iii. Warranty Certificate

15. Tests to be performed at ITER-India site in accordance with Test Matrix by ITER-India for final acceptance.

## 5. Technical Specifications

Detailed specifications of SOM based HVPS controller board are as follows.

**Table 2 Detailed specifications of SOM based HVPS controller board**

| Sr. No. | Descriptions | Details |
|---------|--------------|---------|
| 1 | Input Power Supply | +5V DC |
| 2 | Card Size: | 6U (compatible with existing 6U bin)) |

| 3 | Carrier Board: | Total DIOs: 136 Nos, compatible with existing 6U bin (LVTTL). |
|---|---|---|
| 4 | Front Interfaces | USB-UART, JTAG and Ethernet connector, SD Card, User LEDs, Power Good LEDs (Indicator). |
| 5 | Locking mechanism | Shall have lock with a screw to fit the card in bin |
| 6 | Face plate | Face plate shall be of sturdy material, with Light indicators for all channels; it shall have relevant printed labels |
| 7 | Connector | VPX Connector, compatible with existing Motherboard |
| 8 | Installation | Indoor |
| 9 | Cooling | Forced Air cooled with Provision of fan module for KRIA SOM. |
| 10 | Software | Vivado Node Locked ML Enterprise Edition License for Windows 11 Operating System (Perpetual license in the name of ITER-India) |
| 11 | Testing | As per section 6 tests to be performed |

## 6. Tests to be performed

### a. Visual Inspection

Visual inspection of the SOM based HVPS controller to ensure there is no physical damage, clearances are compliant, proper wiring, labelling etc.

Before functional tests, controller boards shall be visually checked for following,

**Table 3 Parameters for Visual Inspection**

| Sr. No. | Parameter | Observation | comment |
|---|---|---|---|
| | | | |
| 1 | 6U Bin compatible size for SOM based controller board | | |
| 2 | Insertion/withdrawal of controller board to/from the existing 6U bin, it should be smooth.<br><br>Card locking mechanism: card shall have lock with a screw on face plate. | | |
| 3 | Face plate quality, Face plate labels[3]. | | |
| 4 | Mechanical integrity of KRIA SOM board, Carrier Board and Mother board in existing 6U bin | | |

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[3] Information on labels shall be conveyed to supplier during manufacturing phase.

| 5 | Continuity test for power cable and tightness of connectors | | |
|---|---|---|---|

### b. Functional Test

Functional test shall be performed with SOM based HVPS controller board integrated in similar/existing 6U controller bin (signal conditioning unit comprises of Motherboard, 14 No's of TX/RX Boards (10 channels/board)), loopback of 70 Nos of transmitter and receiver channels (preferred simultaneously) with test condition mentioned in Table 4 Test condition and observations. Signal integrity shall be monitored in software (Preferred with logging facility for Crosstalk and Data Corrupt).

Result to be observed for delay, jitter, rise and fall time; maximum acceptable value is mentioned in Table 4 Test condition and observations[4],

Test programs/software shall be developed by Supplier; results shall be observed on HMI / Oscilloscope.

Power turn on/ turn off behaviour of controller board for control signals on DIOs shall be observed.

**Table 4 Test condition and observations**

| | Test condition and observations | | |
|---|---|---|---|
| **Sr. No** | **Specification** | **Values** | **Remark** |
| 1 | Signal frequency (Transmitter – 70 Nos) | 500 Hz to 300kHz | Additional test shall be performed up to 1 MHz |
| 2 | Signal frequency (Receiver – 66 Nos) | 500 Hz to 300kHz | Additional test shall be performed up to 1 MHz |
| 3 | Signal Level (Low/High) | LVTTL | 0V / 3.3V |
| 4 | POF Cable Length Supported | >= 50 meters | |
| 5 | Delay (Between Tx-Rx) | < 500 n sec | With 50m cable |
| 6 | Jitter | < 50n sec | |
| 7 | Rise Time | <100 n sec | |

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[4] Existing 6U bin is qualified for mentioned specifications; it shall be tested for similar specifications with new SOM based controller board.

| 8 | Fall Time | <100 n sec | |
| 9 | Crosstalk and Data Corrupt | | All channels shall be observed for correctness of received data and cross talk/ Pickups from adjacent channels |
| 10 | Delay between two randomly selected receiver channels | < 10 n sec | |
| 11 | Pickup/noise spikes on receiver signal with 1µs delayed signal on two adjacent TX | Check for crosstalk and Error in Data | |

Aim:

1. To verify implemented logic.

All TX channels o/p shall be loop backed to RX i/ps.

All channels should be checked for logic; Channels can be toggled High and Low using buttons on HMI. Status and intensity of LEDs on Tx and Rx cards shall be observed. LED displays on HMI shall also be observed.

**Table 5 To verify implemented logic**

| Tx i/p | LED on TX cards | LED on RX cards | LED on HMI | Comment |
|--------|-----------------|-----------------|------------|---------|
| | | | | |
| Logical High | | | | |
| Logical Low | | | | |

### c. Burn in test

Aim:

1. To observe functional performance of the SOM based HVPS controller board integrated in existing 6U controller bin over the time.
2. To measure power requirement of SOM based HVPS controller board integrated in existing 6U controller bin with full load operation.

Burn in test shall be performed on SOM based HVPS controller board integrated in existing 6U controller bin. Bin shall be functionally ON with loop back of all 136

channels and observed for 8 hours of continuous operation in ambient temperature. <u>Test programs / software shall be provided by supplier</u>; results shall be observed on HMI / Oscilloscope. Signal integrity shall be monitored in software (Preferred with Logging facility for Crosstalk and Data Corrupt).

Keep with all Tx and Rx cards mounted in existing 6U controller bin, with all Tx channels loop backed. Run code-1 so that all Tx channels transmit 300kHz signal. Keep power on for 8 hours of continuous burning and observe received measured frequency at any one selected Rx channel.

Log/Monitor input power drawn from both the DC power supplies by one existing 6U controller bin. Logging can be introduced in software if deemed necessary.

**Table 6 Observation during Burn-in Test**

| Time | Measured Frequency at Rx channel | Power drawn by existing 6U controller bin | | Comment |
|---|---|---|---|---|
| | | 3.3V | 5V | |
| | | | | |
| 0 Hour | | | | |
| 2 Hour | | | | |
| 4 Hour | | | | |
| 6 Hour | | | | |
| 8 Hour | | | | |

After Burn in Test, repeat "Functional Test" and observe the difference.

## 7. Test Matrix

**Table 7 Test Matrix**

| For Prototype (1 No) and Production Units (3 Nos) | | |
|---|---|---|
| Name of Test | At Supplier Site | At ITER-India Site |
| Visual checks | Yes | Yes |
| Functional Test (With reduced Loopback channels) | Yes | **NA** |
| Functional Test (With all Loopback channels) | **NA** | Yes |
| Burn in test | **NA** | Yes |

## 8. Input drawings / documents by ITER-India to Supplier

1. GA/BOM of Existing 6U assembled controller bin
2. Functional test report of Existing 6U assembled controller bin
3. Site Acceptance Test (SAT) Report of Existing 6U assembled controller bin
4. KRIA SOM Product Selection Guide (XMP 499)
5. KRIA SOM Carrier Card Design Guide (UG1091)

## 9. Execution of works

The overall procurement cycle is divided into following phases:

- Detailed/manufacture Design
- Manufacture
- Factory Acceptance Testing
- Delivery to the ITER-India, IPR Site
- Receipt and Physical Verification at the ITER-India, IPR Site
- Site Acceptance at the ITER-India, IPR Site

1) Execution of the scope under this PO shall be governed by the Specifications, terms and conditions provided by ITER-India.

2) Supplier shall develop and manufacture the equipment on the basis of technical inputs provided by ITER-India. Intensive interaction is required between ITER-India & Supplier throughout the work. ITER-India will closely monitor progress at all stages of work: design, manufacture, testing and qualification etc.

3) Supplier shall offer/submit QA reports at all stages of work, to ITER-India. To facilitate inspection by ITER-India, Supplier shall:

- Allow access at all reasonable times during manufacture, assembly and testing to the premises in which the work is carried out.
- Furnish the latest drawings, instruments, testing equipment etc., required for inspecting the job. Prints of all the latest required drawings and approved procedures shall be made available for inspection and retention, if so desired.

## 10. Periodic meeting and reports

Supplier shall provide to ITER-India a bi-monthly progress report on all works under this PO. The report shall be prepared using the standard template.

Progress meetings shall be conducted on regular basis as required upon mutual agreement.

## 11.  Responsibilities

The responsibilities between the Parties is summarised in Table 8 Summary of the Responsibilities between the Supplier and ITER-India.

**Table 8 Summary of the Responsibilities between the Supplier and ITER-India**

| Activity | ITER-India | Supplier |
|---|---|---|
| **Phase 1 Design** | | |
| Submission of design documents/simulations/ datasheets | A | R, D |
| **Phase 2 Manufacture, FAT and Delivery** | | |
| Manufacturing | A | R, D |
| Packing and Delivery to the ITER-India, IPR site | A | R, D |
| Unloading at ITER-India, IPR site | A | R, D |
| **Phase 3 Receipt & Acceptance** | | |
| Receipt and Physical verification | A | R, D |
| Site Acceptance Test at ITER-India, IPR | A | R, D |

R = Responsible for organizing and performing the content

D = Responsible for Demonstration of the content

A = Review/Comment/Accept/Approve

## 12.  Final Acceptance

Final / Site Acceptance of the Items/components will be subject to the fulfilment of requirements given in Technical Specifications. After receiving SOM based HVPS controller boards at ITER-India site, they shall be checked visually for any damage and tested functionally with loopback method in 6U bin. Any defect if found after inspection the same may be reported to the supplier. Acceptance shall be given on completion of successful functional tests or subset of it within 60 days after receiving controller at ITER-India lab.

Supplier shall remain responsible and liable for the ordered items till final acceptance at ITER-India. A visit by supplier's representatives is required for site installation and final acceptance tests.

Note: The Supplier has to carry out Site Work in a protected area and shall strictly follow ITER-India/IPR Security & Safety Protocol during execution of Site Work.

## 13. Technical Compliance Format

**Table 9 Technical Compliance Format**

| Specifications for item name from ITER-India[5] | | Offered specification (to be filled by the bidder) | Remark (to be filled by the bidder) |
|---|---|---|---|
| **Specification** | **Values** | | |
| Signal frequency (Transmitter – 70 Nos) | 500 Hz to 300kHz (Additional test shall be performed up to 1 MHz) | | |
| Signal frequency (Receiver – 66 Nos) | 500 Hz to 300kHz (Additional test shall be performed up to 1 MHz) | | |
| Signal Level (Low/High) | LVTTL (0V / 3.3V) | | |
| POF Cable Length Supported | >= 50 meters | | |
| Delay (Between Tx-Rx) | < 500 n sec | | |
| Jitter | < 50n sec | | |
| Rise Time | <100 n sec | | |
| Fall Time | <100 n sec | | |
| Crosstalk and Data Corrupt | All channels shall be observed | | |

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[5] Functional test shall be performed with SOM based HVPS controller board integrated in similar/existing 6U controller bin, loopback of 70 Nos of transmitter and receiver channels (preferred simultaneously) using SOM based HVPS controller board for mentioned specifications. Test programs/software shall be developed by Supplier; results shall be observed on HMI / Oscilloscope. Power turn on/ turn off behaviour of controller board for control signals on DIOs shall be observed.

| | | | |
|---|---|---|---|
| | for correctness of received data and cross talk/ Pickups from adjacent channels | | |
| Delay between two randomly selected receiver channels | < 10 n sec | | |
| Pickup/noise spikes on receiver signal with 1µs delayed signal on two adjacent TX | Check for crosstalk and Error in Data | | |