ITER-India's response to Pre-bid Query against Tender No. I-ITN21002

Query No.	Ref.: Section of Part-A(II)	Description of the Query	Response of ITER-India
1	1	Frequency range of 35MHz to 60MHz RF samples: Does system operate at fixed frequency or frequency can change anywhere between the range specified?	System will be operated at any frequency between 35 to 60 MHz (RF input frequency band) as per operational requirement. However, the frequency will be changed by ± 1MHz around that operating frequency as bandwidth of RF amplifier is +/- 1MHz.
2	3.1.1	With respect to the sample signals DC1, DC4, DC7 and DC8, what is the dynamic range expected? More than 40dB but how much more?	Dynamic range more than 40dB is acceptable which will be further discussed during design phase.
3	3.1.1	What are the specifications of the phase reference and other reference signals? How are these signals interfaced to connect with the measurement & control module?	Reference signals are 0-10V analog type. These signals are connected through N type cable as defined in section 3.1.1 of tender Part-A(II)
4	3.2.3	We assume close loop response time of 20us is for the overall system. What is the expected response time of the measurement	20us is response time for measurement and control module.
5	2	Is there any requirement for overall power consumption of this module? If yes, please specify.	Appropriate power supply shall be selected for proper functioning of the module. This shall be decided by the
6	2	Will ITER-India provide an existing reference MATLAB model that can be used for developing the amplitude & phase calculation algorithm?	No, MATLAB model will be developed by bidder with help of RF domain expert and submit to ITER-India.
7	3.1.2	Is the mapping between phase change and output 0-10V DC on a linear scale? If not, please provide the details.	Measured phase 0-360 degree is mapped between 0-10V as defined in section-3.1.2 of Tender part-A(II) and it shall be linear.

8	4	Will ITER a provide a test plan for verification of the system as part of the Factory Acceptance Test?	Test plan will be prepared jointly after PO placement and performance will be evaluated against specification defined in section 3.2.4 of Tender part -A:(II)
9	3.1.1	Since the input and output of the module is 0 to 10VDC and processing is in digital domain, why is an FPGA RFSoC recommended? We understand that RF SOC or any other alternate FPGA based solution with external ADCs and DACs can be considered.	RF input signals level are from 10mVp-p to 1Vp-p with minimum 500MSPS sampling rate. Reference input signals are from 0-10V DC. RFSoC is recommended which has inbuilt ADC with high sampling rate and fulfill the specified voltage range.
10	2	What is the expected function of the GUI? What controls & knobs are required on GUI? What interface is desired and expected OS to support?	GUI will be used for conducting FAT and SAT for the module. Amplitude and phase reference and measurement & control signals shall be displayed on the GUI. Windows based OS is suitable for the development platform and Ethernet (TCP/IP) interface is preferred which will be finalized during design phase.
11	3.2.2	We assume prototype manufacturing is part the vendor scope, please confirm. And what is the total number of physical prototypes to be delivered to ITER-India?	Prototype module development is bidder's choice. However, this tender is for development of single module.
12	2	Is the module required to comply with regulatory standards? If yes pl. specifies.	All the components shall be complied industrial grade and electronics components should be RoHS complied. Please refer Section-2-point no.10 of tender Part-A(II).
13	2	Should Mil. grade or Industrial grade components used in the design? Mil. grade has a temperature range of -55degC to +125degC while Industrial grade components have a temperature range of -40degC to +85degC	Industrial grade components will fulfill ITER-India's requirement.
14	3.2	How are the eight output signals: Ch [1-4] Amp and Relative Phase outputs used by the overall control system?	Measured amplitude and relative phase is given in the input of control loops for controlling overall amplitude and phase. It is defined in section-3.2 & Figure-2 and will be Further discussed during design phase.

15	2	Does ITER India have specific tool requirement with respect to the Hardware design? We use either Cadence or Altium for HW and PCB design.	Altium is preferred. Editable executable .pcb file shall be delivered section-2-point no.11
16	2	GUI requirement: will it have only the parameter configuration option and is it required to stream I/Q samples.	Pl. refer answer of query-10
17	3.2	Need detailed equation and internal block diagram for ampl and control loop	Specific transfer function of amplifier system is not available. However, further discussed during design
18	2	Any test vectors (MATLAB or Simulink) be provided to model	Pl. refer answer defined of query -6
19	2	What is the type of interface to PC for GUI.	Pl. refer answer defined of query-10.
20	2	we can use Zynq processor system for both user and config	Yes, further discussed during design phase.
21	3.1.1	Is specified adc/dac width meet overall performance requirement?	Yes, it will fulfill the requirement.
22	3.2	Please update remarks column in table 3.2.4	Section-6 of Part-A(II) shall be properly filled and submitted along with bid and if there is any remark it will be addressed.
23	1	the source for ampl/phase ref signal is mentioned in figure-2 from plant I&C. Pl clarify the term plant I&C and confirm on the source of ref signal	Plant I&C is higher level controller. FAT and SAT will be done with normal FG/Simulated inputs.
24	3.2.1	as per figure-3 equation and section 3.3.2 control loop description	Equations are only reference to measure relative phase which may be used as measurement input for control loop.
25	3.3.2	Xilinx IP shall be used for FPGA design and assuming any format (Verilog/VHDL and encrypted RTL) is ok for this requirement. Pl confirm	Any Xilinx IP may be used. However, license of used IP shall be deliverable to ITER-India as defined in section 3.3.2 of Tender-Part A(II). VHDL is preferred for programming.
26	3.2.4	The parameter mentioned in section 3.2.4 are for standalone unit	During FAT performance is evaluated using normal FG/Simulated inputs only.
27	3.1.1	The ADC sample rate mentioned is on minimum side and it is allowed sample at higher rate if any HW/FPGA PLL limitation during the design phase. Pl confirm	Higher sampling rate can be considered if hardware resources allow.

28	3.1.1	All RF source signals are treated as independent and no phase alignment.	All RF samples are independent as it is taken from different locations of the RF source. However, synchronization input is required to synchronize different modules.
29	3.2.2	When Amplitude of both the channels are to be compared, what is the allowable difference between these two?	Resolution of measurement for amplitude shall be better than 0.1dB and hence, allowable difference in measurement of amplitude for different channel must be ≤0.1 dB maximum.
30	3.2.3	When Phases of both the channels are to be compared, what is the allowable tolerances between these two?	Resolution of measurement for phase should be better than 0.5 degree and hence, allowable difference in measurement of phase for different channel must be ≤ 0.5 degree.