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Title	Tender No. I-ITN21002 dated 23rd September, 2021 for Development of FPGA (Field Programmable Gate Arrays) based RF Control System for RF Source
Sub-title	Part-A(II): Scope of Supply & Work, Technical Specifications and Drawings

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Contents

Abbreviations

ADC – Analog to Digital Conversion
BOM - Bill of Material
DAC – Digital to Analog Conversion
DC – Directional Coupler
DDC – Digital Down Conversion
EMC - Electro Magnetic Compatibility
EMI - Electro Magnetic Interference
FAT - Factory Acceptance Test
FG – Function Generator
FIR – Finite Impulse Response
FPGA – Field Programmable Gate Arrays
GUI – Graphical User Interface
HPA – High Power Amplifier
I&Q – In-phase & Quadrature-phase
ICH&CD - Ion Cyclotron Heating & Current Drive
II -ITER-India
IIR – Infinite Impulse Response
IO - ITER Organization
IPR – Institute for Plasma Research
kW – Kilowatt
LCU – Local Control Units
LED - Light Emitting Diode
MSPS – Mega Samples Per Second
MW - Megawatt
OEM – Original Equipment Manufacturer
QP – Quality Plan
RF Source - Radio Frequency Source
RFSoC – Radio Frequency System-on-Chip
SAT - Site Acceptance Test
SMPS - Switch Mode Power Supply
SSPA - Solid State Power Amplifier

1 Introduction

Ion Cyclotron Heating and Current Drive (ICH&CD) package is responsible to develop RF source having capability to generate RF power 2.5MW/VSWR 2.0/2000sec in the frequency range of 35-61MHz. This includes high power tube-based amplifiers (3 stages of cascaded RF amplifiers – SSPA, HPA2, HPA3), different auxiliary power supplies with high voltage/high current ratings and independent data acquisition & control system.

The critical requirement for RF source is to control /maintain amplitude and phase of RF output. Figure-1 shows the typical block diagram of RF source having indication of measurement point in RF source. Directional couplers (DC) are mounted in the output of each amplifier stages of the RF source to extract RF samples from different locations for measurement purpose. Critical locations for measurement of RF amplitude and phase of forward samples are DC1, DC4, DC7 and DC8 as shown in figure-1. These signals will be used in Digital I&Q based technique for detection of amplitude and phase of RF sample, which is explained in section - 3.2. RF detectors are mounted on each directional coupler for converting RF samples to DC output voltage which corresponds to forward power and reflected power.

The scope of this tender is to develop measurement & control module for amplitude and phase. Here, Digital I&Q based technique is selected where Digital down conversion (DDC) and appropriate decimation process will be considered for optimize the sample of I & Q for calculation of amplitude & phase. It is proposed to use FPGA RFSoC module for design and development of RF measurement and control algorithm to fulfill the requirement.

RF detectors and corresponding measurement scheme is out of scope for this tender.

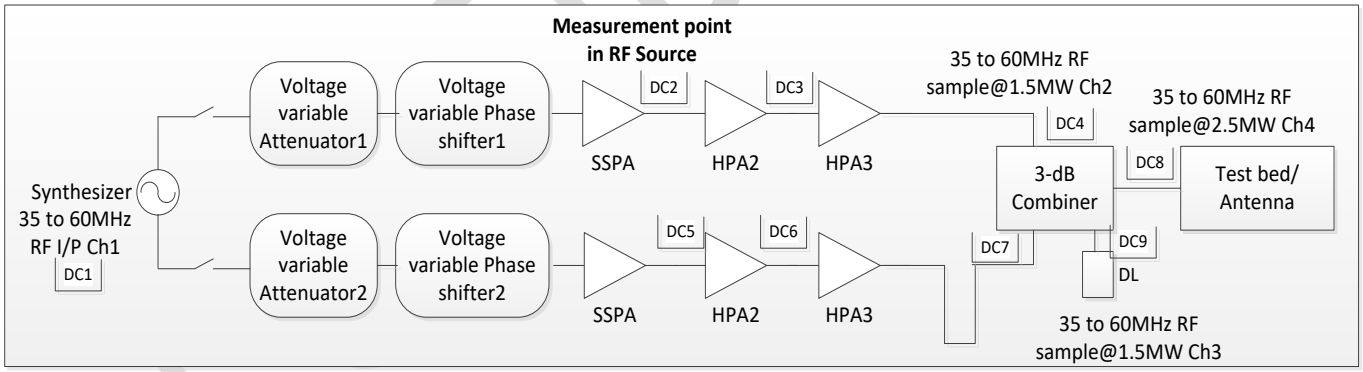

Figure 1: Typical block diagram for RF Source

Figure 2 shows the block diagram of Digital I&Q based RF measurement and control technique in brief.

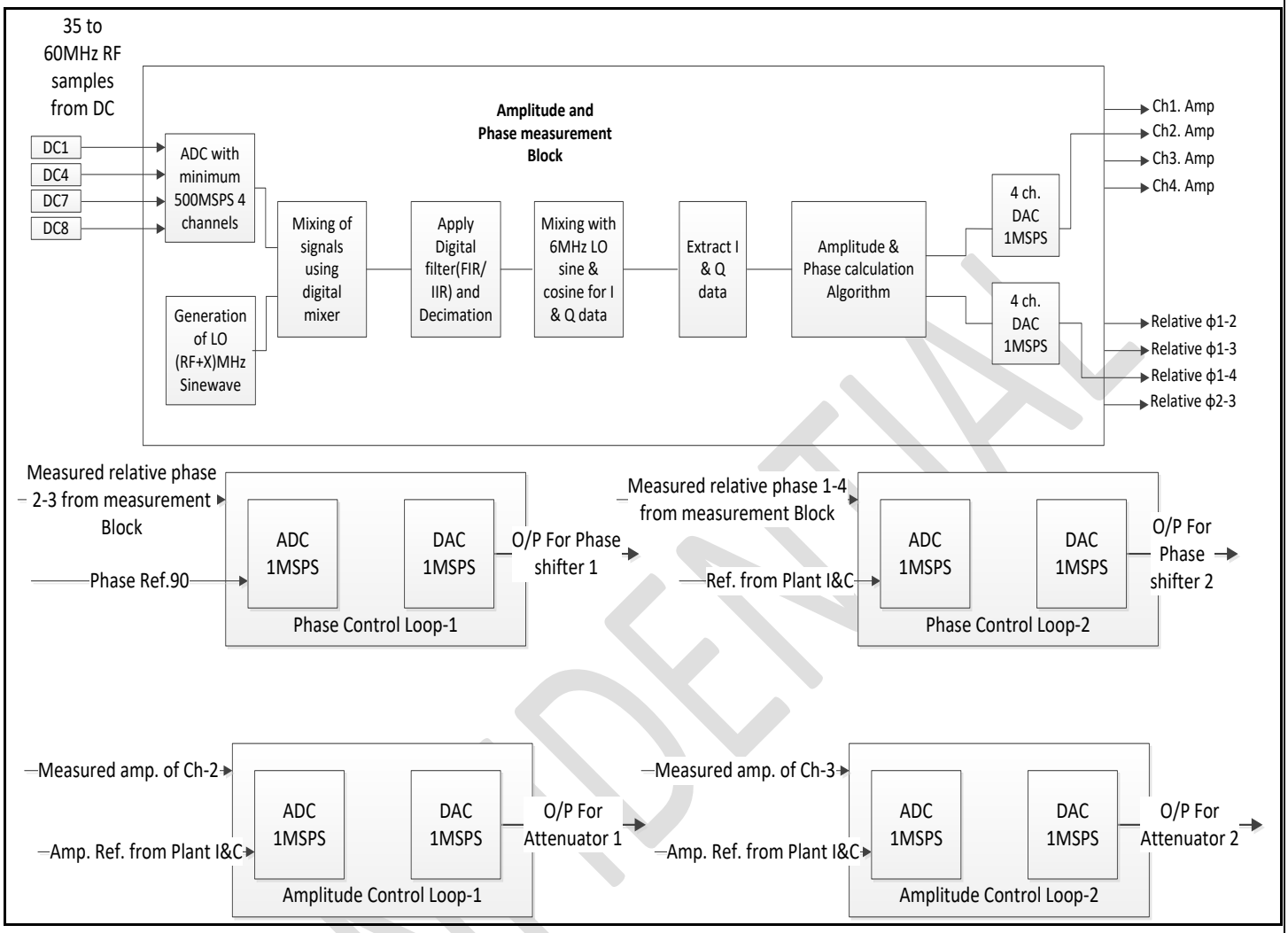

Figure 2: Block diagram for RF measurement and control technique

2 Scope of Work

Bidder shall:

1. Prepare Quality plan, Manufacturing & inspection plan, Packing & transportation plan, Activity schedule and submit the same at the time of kick off meeting for II approval.
2. Finalize appropriate FPGA based RFSoC module or equivalent module as per specification defined in section-3.
3. Procure the FPGA based RFSoC/equivalent module after getting approval from II.
4. Develop hardware & software architecture for this project and submit the same for II review.
5. Generate technical document as defined in Section 3.3.1, Table-4: Sr.No.4 and submit the same for II-approval.
6. Generate BoM and submit the same for II review and procure the material.
7. Procure Appropriate DC power supply (preferable make: Siemens, XP, Schneider, Meanwell or equivalent) and other accessories required for proper functioning of the proposed system.
8. Procure required low loss, phase stable RF coaxial cables – ST-142 (2 meter each) for input and output connections and supply the same along with system.
9. Procure 19" rack mountable EMI/EMC compatible enclosure with proper height and depth (not more than 4U-height & 450mm depth), mount the selected FPGA module & Power supply module in this enclosure and make internal wiring for proper interface with field signal as well as operational/developmental console.
10. PCB layout shall be designed to fulfill EMI/EMC guidelines and simulated for the same. Simulation results shall be submitted for II review.
11. Submit schematic diagram, PCB layout and Gerber files of all the custom-built PCB which is used to develop this module.
12. Develop code for digitizing RF signal (35-61MHz) at appropriate frequency for further processing for measurement & control of RF amplitude & phase.
13. Develop code for digital signal processing to measure amplitude, phase & frequency and generate 0-10V signal corresponding to amplitude & Phase of each RF input and frequency for RF output measured at directional coupler-8.
14. Develop appropriate Feedback & feedforward control loop for Amplitude & phase control loop as described in section - 3.2.
15. Develop acceptance test plan as per section - 4 and submit the same for II approval.
16. Develop GUI for proper demonstration of defined functionality and submit the editable software code.
17. Submit list of software package used for development and procure the license version of the same & deliver the same along with hardware.
18. Conduct FAT & SAT in presence of II's representative as per mutually agreed test procedure, generate reports and submit the same for II approval.
19. Deliver all source code & firmware (editable) developed during execution of this project.
20. Generate operational, Installation, maintenance & service manual and submit the same for II-review and final acceptance. Installation manual shall contain Installation, configuration, start-up and shut down procedure.
21. Submit all the certificates & technical data sheet / user manual of procured hardware in hard copy as well as in soft copy.

22. Provide training of 10 days to two II-Engineers for used software package during development of this project.
23. Packaging and transportation to ITER-INDIA is bidder's responsibility. Bidder need to use adequate packing material (antistatic bags) for packaging the items for damage free transportation. Bidder is responsible for any damage to the items during transportation and the damaged item will be replaced by the bidder free of cost within mutually agreed time.
24. Provide support of technical man-power at site, to resolve any issues if arise during integration of RF measurement & control module with actual system. However, the responsibility of performance of integrated system will lies with ITER-India.

3 Technical Specification

This section describes the detailed technical specification of RF measurement and control module. It also describes proposed RF measurement and control scheme for amplitude and phase of RF source along with specification of amplitude and phase control loop.

3.1 Major Technical Specification of RF measurement & control module:

3.1.1 Input specification

1. Frequency: 36-60MHz (+/-1MHz bandwidth)
2. Dynamic input range of amplitude: more than 40dB {10mVp-p to 1Vp-p (maximum)}
3. ADC:
    a. 14-bit with 500MSPS (Minimum) for RF samples (4 channels)
    b. 14-bit with 1MSPS (Minimum) for reference signals (4 channels)
4. Input Impedance: 50Ω
5. Input connector: N type (Female)
6. Input supply: Single phase 230V/50Hz

3.1.2 Output specification

1. DAC: 12-bit with 1MSPS (Minimum) for all analog output
2. Output of amplitude: 0-10V (4 channels)
3. Output of relative phase: 0-10V corresponds to 0-360 degree (4 channels)
4. Output for Amplitude control loop (Attenuator1&2): 0-10V (2 channels)
5. Output for Phase control loop (Phase shifter 1&2): 0-10V (2 channels)
6. Output connector: BNC type (Female)

3.1.3 Specification for RF module rack

1. 19” rack mountable EMI/EMC compatible module.
2. Height: Maximum 4U
3. Depth: Maximum 450 mm

3.2 RF Measurement & control scheme

Main Specification of RF source are as follow for reference:

- Operating Frequency range: 35-60 MHz
- Bandwidth of the system: +/- 1MHz (Real time change as per experimental requirement)
- Source o/p power: 2.5MW for 2000s for matched load to VSWR 2:1 condition
- Each chain o/p power: 1.5MW for 2000s for matched load to VSWR 2:1 condition
- Overall gain of each cascaded chain of amplifiers: ~92dB

As shown in figure-3, synthesizer is used to feed the signal to attenuator & phase shifter control block and output of this control block is used to drive cascaded chain of amplifiers. Such two chain is combined using combiner to get final out put which will be connected to test load (having capability to vary load impedance for VSWR 2:1) or to antenna for dumping the power to tokomak plasma.

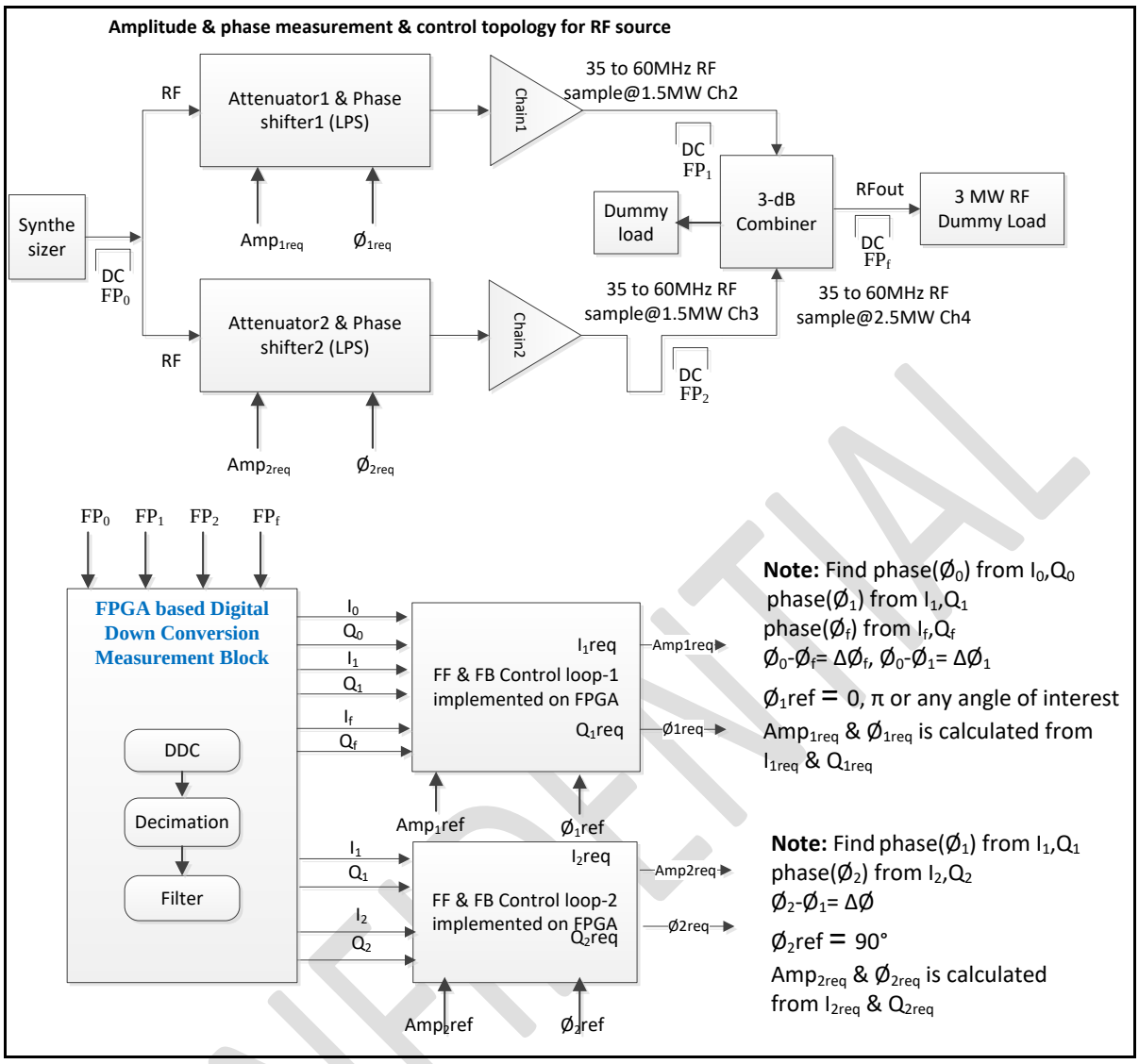

Figure 3: Amplitude & phase measurement and control topology

Requirement: Project requirement is to control/maintain amplitude and phase of RF output. For measurement & control of amplitude and phase, Digital I&Q based technique is considered where Digital down conversion (DDC) and appropriate decimation process will be considered, which is described in lower part of Fig.-3.

3.2.1 Amplitude and phase measurement:

The amplitude and phase of RF signal is measured using Digital Down Conversion methodology where RF samples received from directional coupler are directly digitized using ADC. After digitizing, digital signal processing should be carried out for getting amplitude & phase value and converting them to get 0-10V DC signal for acquisition. Same signals will be used as measured signal at one of the inputs of amplitude and phase control loops. As this measurement technique requires substantial amount of FPGA resources, only critical location (FP_0, FP_1, FP_2 & FP_f which are sampled using DC1, DC4, DC7 and DC8 respectively) for RF measurement is considered which are shown in figure-3.

3.2.2 Amplitude control loop:

Each RF source consists of two chain of amplifier; hence two amplitude control loops is envisaged for each RF source to maintain desired output power from each chain of amplifier. Individual set point for each chain of amplifier is generated locally by control system and connected with this module as an electrical signal (0-10V).

Each local control loop will maintain the o/p by generating proper Amp_{1req} and Amp_{2req} signal to control the attenuator - 1 and attenuator - 2 respectively.

3.2.3 Phase Control loop:

In each source, two phase control loops will be incorporated. One of this control loops is used to maintain the phasing of individual source RF output with respect to phase reference provided by main controller. Second control loop is used to maintain required phase (as per operating frequency ~90°) in between the outputs of two chains of amplifiers, which are connected at the input of the 3dB Hybrid combiner.

Phase control loop for Individual Source:

Phase references of 0-10V DC for individual source is generated by main controller. Measurement block take the RF samples as FP_0, FP_1, FP_2 & FP_f and digitized by 4-channel digitizer for further processing to get I, Q corresponding to each RF signal.

Control loop1 is responsible to change/maintain the phase requirement of individual source output and hence it will calculate relative phase between FP_0 & FP_1 ($\Delta\varnothing_1$) and FP_0 & FP_f ($\Delta\varnothing_f$) and then try to maintain $\Delta\varnothing_f$ as requested by main controller. For that, control loop 1 generates $\varnothing_{1req}$ signal to control the phase shifter1 connected in chain-1.

Phase control loop for 3dB Hybrid combiner:

To maintain a predefined phasing (~90°) between two inputs of the 3-dB Hybrid combiner, control loop2 is used and hence it will calculate relative phase between FP_1 & FP_2 ($\Delta\varnothing$) and then generates phase reference corresponding to required phase as per operating frequency. Corresponding to this phase reference, $\varnothing_{2req}$ is generated to control the phase shifter2 connected in chain-2.

3.2.4 Desired control loop specifications are as follows:

Table 1: Specification for Amplitude control loop

Sr.No.	Parameter	Specification	Remarks
1	Forward power control range	0.005 to 3.5 MW	
2	Power modulation accuracy	5.0 %	

3	Response time for amplitude control loop from half power to full power	1 ms	
4	Response time for amplitude control loop from zero power to full power	10 ms	
5	Response time against trip request	<10 µs	
6	Overshoot	<5%	
7	Max residual power with RF power source ready (power reference at 0)	2.0 kW	

Table 2: Specification for phase control loop

Sr.No.	Parameter	Specification	Remarks
1	Phase control range	0-360 degree	
2	Minimum output power level allowing phase control	5 kW	
3	Absolute phase accuracy, including offset and noise	1 degree	
4	Closed loop response to a phase step (≤90°)	20 µs	
5	Phase overshoot	< 20 degree	

3.3 List of Deliverables

3.3.1 Documents

Bidder shall be responsible to generate necessary required documents as defined in table-3. Bidder needs to submit the same for review and approval from II. Final copy of the documents shall be submitted in softcopy as per specified format along with hardcopy (where applicable).

Table 3: List of deliverable documents

Sr. No	**Description**	**Details**	**Format for document**	**Remarks**

1	Quality related documents	Quality plan, Manufacturing & inspection plan, Packing & transportation plan, and Activity schedule in softcopy as well as one hardcopy.	PDF/XLSX	In USB drive
2	BOM containing name of supplier and part number	Bill of material in softcopy as well as one hardcopy.	XLSX (MS-Excel)	In USB drive
3	Technical Documentation	• Engineering Design Document which describes hardware and software architecture • Detailed description of firmware BSP and software used for this project • Editable version of schematic design, PCB layout, Gerber file and all other relevant design file for custom-built PCB • Installation & Configuration Manual including start-up and shut down procedure • Operational, Service & Maintenance Manual (Softcopy as well as one hardcopy)	DOCX & PDF	In USB drive
4	FAT & SAT	Final acceptance test plan, Factory Acceptance Test report and Site Acceptance Test report in softcopy as well as one hardcopy.	DOCX & PDF	In USB drive
5	Certification	Certificate/Manual provided by OEM in hardcopy.	PDF	In USB drive

3.3.2 Hardware and software items

Bidder shall be responsible for delivering the hardware listed in table-4.

Table 4: List of Hardware & software items

Sr. No	Description	Qty	Remarks
1	FPGA based RFSoC/equivalent module & required DC power supply mounted in 19" EMI/EMC compatible enclosure	1 set	
2	Low loss, phase stable RF cables – ST-142 (patch cords of minimum 2-meter length) for input and output connections	25 Nos	
3	Licensed version of Software module required for development & testing	1 set	
4	Editable source code of final Application along with Board Support Packages and firmware along with its executable file	1 set	
5	Editable version of source code developed for GUI or other module for performance evaluation of the board	1 set	

4 Acceptance Criteria

FAT and SAT procedures defined here is for reference. Final and detailed version of FAT & SAT procedures will be prepared by bidder and submitted to II after 3 months of PO placement, for final approval.

4.1 Factory Acceptance Test

The following tests will be done at factory site.

- Basic performance of hardware will be checked.
- Wiring & Interface point will be checked.
- Amplitude measurement & phase measurement will be checked using RF signal generated from FG.
- Logic of Amplitude control loop & phase control loop will be checked through simulated signal or simulator.

4.2 Site Acceptance Test

The following tests will be carried out during SAT:

- Operational procedure including Installation, configuration, start-up and shut down procedure will be checked.
- Interface point will be checked and connected with actual component/sub-system/system like attenuator, phase shifter and directional coupler.
- Amplitude & phase measurement will be checked with simulated signal.
- Amplitude & phase control loop will be checked for its performance as defined in section - 3.2.
- Amplitude & phase measurement will be observed and recorded with actual RF signal.
- Bidder shall prepare Site Acceptance Test report and submit to ITER-India for acceptance.
- ITER-India will provide test facilities like, power (230V AC), space and equipments like, Spectrum analyser, function generator, oscilloscope, multimeter etc.

5 General Instructions for Bidder

1. Bidder shall submit scope understanding document and technical description of execution process of this project along with bid. Technical description document shall include complete block level design with all details including identification of components/sub-modules, interfaces and required power supply which are necessary for development of this project.
2. Bidder shall submit the available resources (design tool used for this project, manpower having experience in development of High-end FPGA module) along with bid.
3. Bidder shall respect the Intellectual property right clause as bidder shall not disclose any information gathered throughout this project or cannot use it without prior permission of ITER-India. ITER-India will be owner of Hardware architecture and source code developed during this project.
4. Internal technical review meeting shall generally be held bi-weekly between ITER-India members and Bidder personnel in form of remote participation.
5. Progress meeting shall be held in-person/remote on regular monthly basis to discuss different technical issue between ITER-India coordinator and Bidder.
6. Progress report shall be submitted on monthly basis to ITER-India.
7. Access to ITER-INDIA deputed representative should be allowed by bidder during technical evaluation and execution of the project.
8. ITER-India Quality officer may visit the factory where work is carried out and he/she may inspect all/any related document.
9. All the necessary test equipment and required power supply will be arranged by the bidder to perform pre-FAT and FAT.
10. All required instruments, accessories, cables and other than deliverable bill of materials for satisfactory demonstration of the system for SAT is to be listed and submitted to II before 1 month of SAT. Those items not listed, shall be provided by the Bidder to conduct SAT.
11. Training shall be arranged during SAT.
12. Final acceptance shall be given after successful completion of training and Site Acceptance test by bidder at II lab, IPR.
13. All documentation shall be in English language only.
14. The bidder shall be responsible for all expenses of their manpower's travel/visit for testing/meeting at any other lab/offices outside their premises.

6 Technical Compliance Matrix

Bidder should be filling the following tables for understanding of technical requirement of this tender.

Table 5: Compliance for Scope understanding

Sr. No.	Requirement as per enquiry	Compliance statement by Bidder	Remarks
1	Scope of work as defined in section - 2		
2	Major technical specification of RF measurement module as defined in section - 3.1		
3	RF measurement & control scheme as defined in section - 3.2		
4	Acceptance criteria as defined in section - 4		
5	General Instructions as defined in section - 5		

Table 6: Technical compliance against documents deliverables

Sr. No	Description	Details	Format for document	Bidder Compliance	Remarks
1	Quality related documents	Quality plan, Manufacturing & inspection plan, Packing & transportation plan, and Activity schedule in softcopy as well as one hardcopy.	PDF/XLSX		In USB drive
3	BOM along with make and supplier	Bill of material in softcopy as well as one hardcopy.	XLSX (MS-Excel)		In USB drive
4	Technical Documentation	• Engineering Design Document which	DOCX & PDF		In USB drive

		describes hardware and software architecture • Detailed description of firmware BSP and software used for this project • Editable version of schematic design, PCB layout, Gerber file and all other relevant design file for custom-built PCB • Installation & Configuration Manual including start-up and shut down procedure • Operational, Service & Maintenance Manual (Softcopy as well as one hardcopy)			
6	FAT & SAT	• Final acceptance test plan Factory Acceptance Test report and Site Acceptance Test report in softcopy as well as one hardcopy.	DOCX & PDF		In USB drive
7	Certification	Certificate/Manual provided by OEM in hardcopy.	PDF		In USB drive

Table 7: Technical compliance for Hardware & software deliverables

Sr. No	Description	Qty	Bidder Compliance	Remarks
1	FPGA based RFSoC module & required DC power supply mounted in 19" EMI/EMC compatible enclosure	1 set		
2	Low loss, phase stable RF cables – ST-142 (patch cords of minimum 2-meter length) for input and output connections	25 Nos		
3	Licensed version of Software module required for development & testing	1 set		
4	Editable source code of final Application along with Board Support Packages and firmware along with its executable file	1 set		
5	Editable version of source code developed for GUI or other module for performance evaluation of the board	1 set		

Authorized Signature by Bidder along with seal and date